LH5101

CMOS 1K (256 × 4) Static RAM

FEATURES

- 256 × 4 bit organization
- Access time: 300 ns (MAX.)
- Low-power consumption:
  Operating: 137.5 mW
  Standby: 55 μW
- Single +5 V power supply
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Two Chip Enables for ease of use
- CE_2 signal enables the device to operate on a minimum standby current
- Data retention is possible with low supply voltage (2.0 V)
- Pin-to-pin equivalent to the Intel 5101
- Package: 22-pin, 300-mil DIP

DESCRIPTION

The LH5101 is a static RAM organized as 256 × 4 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

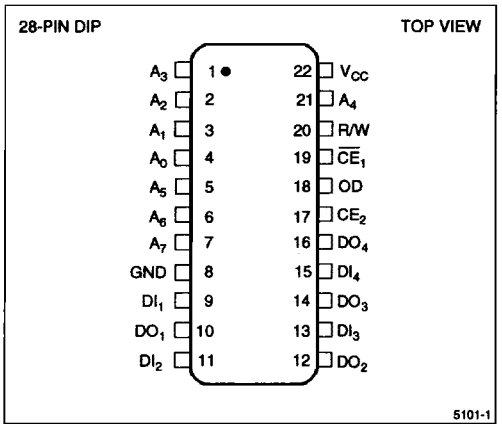


Figure 1. Pin Connections for DIP Package

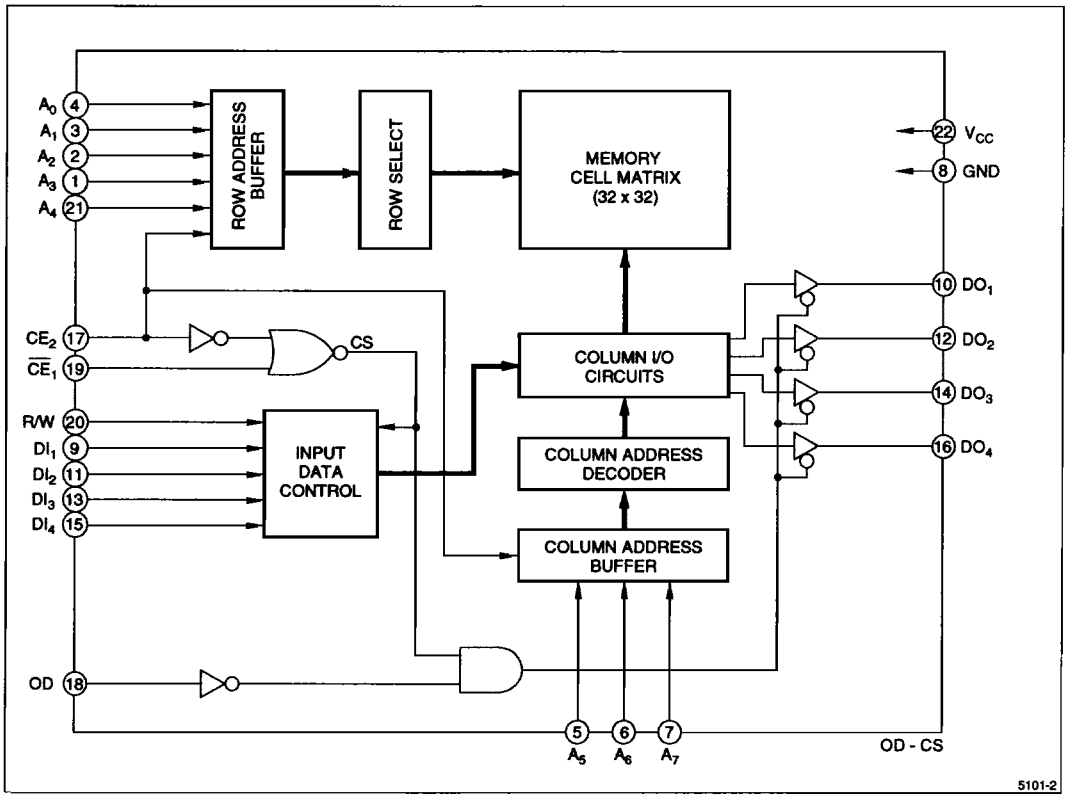


Figure 2. LH5101 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_7	Address input
DI_1 - DI_4	Data input
DO_1 - DO_4	Data output
R/W	Read/write Enable input
$\overline{CE}_1$	Chip Enable input 1

SIGNAL	PIN NAME
$\overline{CE}_2$	Chip Enable input 2
OD	Output disable
V_{CC}	Power supply
GND	Ground (0 V)

TRUTH TABLE

$\overline{CE}_1$	CE_2	OD	R/W	D_{IN}	OUTPUT	MODE
H	X	X	X	X	High-Z	Deselect
X	L	X	X	X	High-Z	Deselect
X	X	H	H	X	High-Z	Output deselect
L	H	H	L	X	High-Z	Write
L	H	L	L	X	D_{IN}	Write
L	H	L	H	X	D_{OUT}	Read

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V	1
Output voltage	V_{OUT}	-0.3 to V_{CC} + 0.3	V	1
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

DC CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = 5 V ±10%)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input 'LOW' voltage	V_{IL}				0.65	V
Input 'HIGH' voltage	V_{IH}		2.2			V
Output 'LOW' voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V
Output 'HIGH' voltage	V_{OH}	I_{OH} = -1.0 mA	2.4			V
Input leakage current	$\|I_{LI}\|$	V_I = 0 V to V_{CC}			1.0	µA
Output leakage current	$\|I_{LO}\|$	V_I = 0 V to V_{CC}, $\overline{CE}_1$ = 2.2 V			1.0	µA
Operating current	I_{CC1}	Outputs open, V_I = V_{CC}, $\overline{CE}_1$ = 0.65 V			20	mA
	I_{CC2}	Outputs open, V_I = 2.2 V, $\overline{CE}_1 \leq$ 0.65 V			25	mA
Standby current	I_{SB}	V_I = 0 V to V_{CC}, $\overline{CE}_2$ = 0.2 V			10	µA

AC CHARACTERISTICS

(1) READ CYCLE (T_A = 0 to 70°C, V_{CC} = 5 V ±10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Read cycle time	t_{RC}	300			ns
Address access time	t_{AA}			300	ns
Chip enable access time 1	t_{CO1}			250	ns
Chip enable access time 2	t_{CO2}			350	ns
Output disable to output	t_{OD}			180	ns
Data output to high-Z state	t_{DF}			100	ns
Previous read data valid with respect to address change	t_{OH1}	0			ns
Previous read data valid with respect to chip enable	t_{OH2}	0			ns

(2) WRITE CYCLE (T_A = 0 to 70°C, V_{CC} = 5 V ±10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Write cycle time	t_{WC}	300			ns
Chip enable (CE_1) to end of write	t_{CW1}	250			ns
Chip enable (CE_2) to end of write	t_{CW2}	250			ns
Address valid time	t_{AW}	60			ns
Data valid to end of write	t_{DW}	150			ns
Data hold time	t_{DH}	40			ns
Write recovery time	t_{WR}	40			ns
OD setup time	t_{OD}	100			ns

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.65 V to 2.2 V
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load condition	1TTL + 100 pF

DATA RETENTION CHARACTERISTICS [1]

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$V_{CE2} \leq 0.2$ V	2.0			V	
Data retention current	I_{CCDR}	$V_{CE2} \leq 0.2$ V, $V_{CCDR} = 2.0$ V			10	µA	
Chip disable to data retention	t_{CDR}		0			ns	
Recovery time	t_R		t_{RC}			ns	2

NOTES:
1. In the data hold mode, voltage on any I/O pin should be lower than V_{DR}.
2. t_{RC} = Read cycle time

CAPACITANCE (f = 1MHz, T_A = 25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	$V_{IN} = 0$ V		3.5	6	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O} = 0$ V		9	12	pF

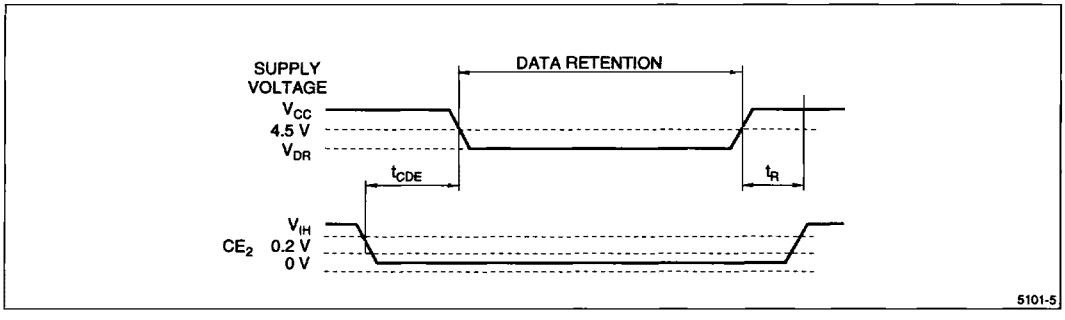
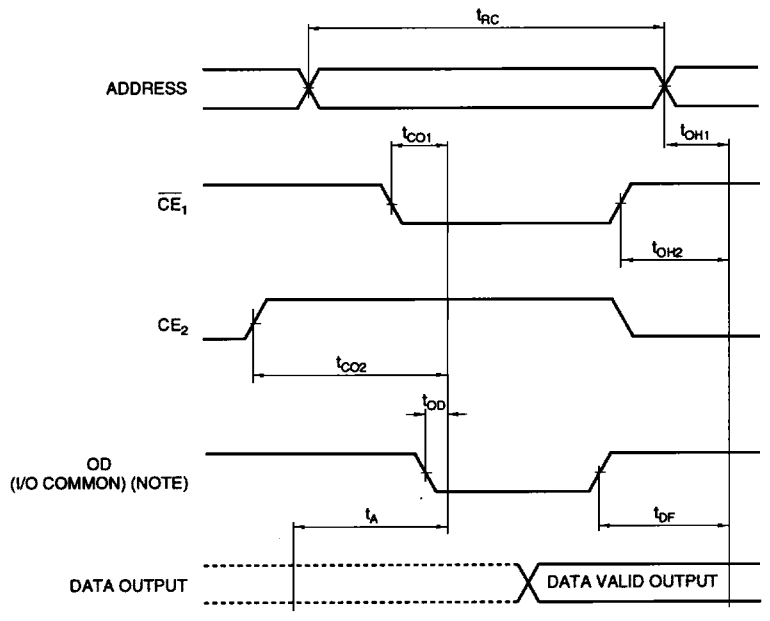


Figure 3. Low Voltage Data Retention



NOTES:
1. When data input and output are separately used, OD should be LOW.
2. During read cycle, R/W should be HIGH.

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Figure 4. Read Cycle

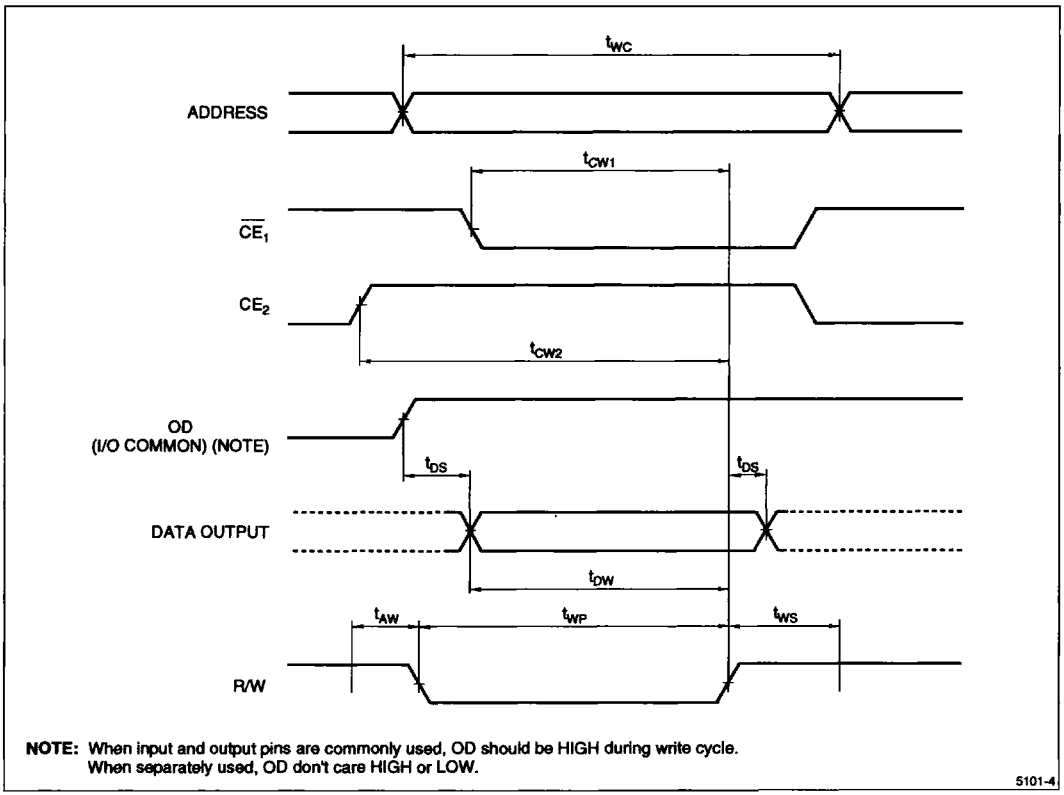

Figure 5. Write Cycle

ORDERING INFORMATION